What is claimed is:

1. A method for fabricating a two layer, storage node electrode, for a DRAM device, on a semiconductor substrate, comprising the steps of:

providing a transfer gate transistor, on said semiconductor substrate;

forming a conductive plug, in a storage node contact hole, with said conductive plug contacting underlying source/drain region, of said underlying transfer gate transistor;

forming a storage node electrode shape, comprised of a first conductive layer, with said storage node electrode shape contacting underlying conductive plug;

forming a metal silicide layer on said first conductive layer of said storage node electrode shape;

converting said metal silicide layer, to an agglomerated metal silicide layer, on said first conductive layer, of said storage node electrode shape, resulting in said two layer, storage node electrode, comprised of said agglomerated metal silicide layer, on said first conductive layer.

2. The method of claim 1, wherein said storage node contact hole is formed in a silicon oxide layer, via anisotropic RIE procedures, using CHF_3 as an etchant.

3. The method of claim 1, wherein said conductive plug is tungsten, formed in said storage node contact hole, via deposition of tungsten, using LPCVD procedures, followed by removal of unwanted tungsten using CMP procedures.

4. The method of claim 1, wherein said storage node electrode shape, is a cylindrical shape.

5. The method of claim 1, wherein said first conductive layer, used for formation of said storage node electrode shape, is an N type doped, polysilicon layer, obtained using an LPCVD procedure, and in situ doped during the LPCVD procedure, or doped via an N type, ion implantation procedure, applied to an intrinsically deposited, polysilicon layer.

6. The method of claim 1, wherein said metal silicide layer is a titanium disilicide layer, obtained via deposition of a titanium layer, using r.f. sputtering procedures, and converted to said titanium disilicide layer via a first RTA procedure, at a temperature between about 400 to 750°C for a time between about 30 to 90 sec.

7. The method of claim 1, wherein said metal silicide layer is a cobalt disilicide layer.

8. The method of claim 1, wherein said agglomerated metal silicide layer, is an agglomerated titanium disilicide layer, obtained via a second RTA procedure, applied to said titanium silicide layer, at a temperature between about 800 to 1000°C, for a time between about 30 to 90 sec.

9. A method of fabricating a capacitor structure, for a DRAM cell, on a semiconductor substrate, featuring a storage node electrode, comprised of a agglomerated titanium disilicide layer, on an underlying polysilicon layer, comprising the steps of:

providing a transfer gate transistor, on said semiconductor substrate, comprised of a polysilicon gate structure on a gate insulator layer, and source and drain regions, in said semiconductor substrate, in regions of said DRAM cell not covered by said polysilicon gate structure;

depositing a first insulator layer;

opening a storage node contact hole in said first insulator layer, exposing top surface of said source and drain region;

depositing a conductive layer on top surface of said first insulator layer, and completely filling said storage node contact hole;

removing said conductive layer from the top surface of said first insulator layer, forming a conductive plug in said storage node contact hole;

depositing a first polysilicon layer;

depositing a second insulator layer;

patterning of said second insulator layer, and of said first polysilicon layer, to form an insulator mesa overlying, a first polysilicon shape, with said insulator mesa comprised of said second insulator layer, and with said first polysilicon shape, comprised of said first polysilicon layer, contacting underlying, said conductive plug;

depositing a second polysilicon layer;

anisotropic etching of said second polysilicon layer, to form polysilicon spacers on the sides of said insulator mesa, and on the sides of said first polysilicon shape;

removing said insulator mesa from underlying, said first polysilicon shape, resulting in a cylindrical, polysilicon storage node electrode shape, comprised of said polysilicon spacers, extending upwards from said first polysilicon shape;

depositing a titanium layer;

a first rapid thermal annealing procedure converting said titanium layer, on said cylindrical, polysilicon storage node electrode shape, to a smooth titanium disilicide layer, while leaving said titanium layer, on the top surface of said second insulator layer, unreacted;

removing said titanium layer from the top surface of said first insulator layer;

a second rapid thermal annealing procedure converting said smooth titanium disilicide layer to said agglomerated titanium silicide layer, resulting in said storage node electrode, comprised of said agglomerated titanium disilicide layer, on said cylindrical, polysilicon storage node electrode shape;

forming a capacitor dielectric layer on said storage node electrode; and

forming a cell plate electrode, for said capacitor structure.

10. The method of claim 9, wherein said conductive plug is comprised of either tungsten, tungsten silicide, or polysilicon.

11. The method of claim 9, wherein said first polysilicon layer is deposited using LPCVD procedures, and in situ doped during deposition, via the addition of arsine, or phosphine, to a silane ambient, or said first polysilicon layer is deposited intrinsically, and doped via ion implantation of arsenic or phosphorous.

12. The method of claim 9, wherein said second insulator layer is a BPSG or PSG layer, deposited using LPCVD or PECVD procedures.

13. The method of claim 9, wherein said second polysilicon layer is deposited using LPCVD procedures, and in situ doped during deposition via the addition of arsine, or phosphine, to a silane ambient, or said second polysilicon layer is deposited intrinsically and doped via ion implantation of arsenic or phosphorous.

14. The method of claim 9, wherein said polysilicon spacers are formed via an anisotropic RIE procedure, applied to said second polysilicon layer, using Cl_2 as an etchant.

15. The method of claim 9, wherein said insulator mesa is removed using a HF vapor procedure.

16. The method of claim 9, wherein said titanium layer is deposited using an r.f. sputtering procedure.

17. The method of claim 9, wherein said first RTA procedure, used to convert said titanium layer to said smooth titanium disilicide layer, is performed at a temperature between about 400 to 750°C, for a time between about 30 to 90 sec.

18. The method of claim 9, wherein said second RTA procedure, used to convert said smooth titanium disilicide layer to said agglomerated titanium disilicide layer, is performed at a temperature between about 800 to 1000°C, for a time between about 30 to 90 sec.

19. A semiconductor capacitor structure, comprising:

a lower electrode, comprising a silicon layer, and an overlying metal silicide layer, covering said silicon layer, wherein said metal silicide layer has a rough surface;

a capacitor dielectric layer over the rough surface of said metal silicide layer; and

an upper electrode, covering said capacitor dielectric layer.

20. The semiconductor capacitor structure of claim 19, wherein said silicon layer comprises vertical polysilicon shapes connected by a horizontal polysilicon shape.

21. The semiconductor capacitor structure of claim 19, wherein said metal silicide layer is selected from the group consisting of titanium silicide, cobalt silicide, nickel silicide, and platinum silicide.